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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/518,772	08/01/2005	Christopher Rodd Speirs	CH02 0021 US	4888
65913	7590	12/14/2007	EXAMINER	
NXP, B.V.			ABDIN, SHAHEDA A	
NXP INTELLECTUAL PROPERTY DEPARTMENT			ART UNIT	PAPER NUMBER.
M/S41-SJ			2629	
1109 MCKAY DRIVE				
SAN JOSE, CA 95131				
NOTIFICATION DATE		DELIVERY MODE		
12/14/2007		ELECTRONIC		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/518,772	SPEIRS ET AL.	
	Examiner	Art Unit	
	Shaheda A. Abdin	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 01 August 2005.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-12 is/are pending in the application.
 - 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-12 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) .
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. The amendment filed on 10/24/2007 has been entered and considered by examiner.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-3, 5-7, 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over He et al. (US. Patent No: 6323849 B1) in view of Duwaer et al (US Patent No: 4922240).

(1) Regarding claim 9:

A row driver circuit (140) for controlling n rows (141-149) of a display device (150) that is operable in a partial mode (column 1, lines 53-61), the row driver circuit (140) having n outputs (i.e. outputs to the rows 141-149), with a logic function (i.e. 110 having logic zero), wherein the logic function deactivates/activates the row outputs in dependence on the partial mode responsive to a first control signal.

Note that He teaches the logic function (i.e. 110 having logic zero) but He does not teach the logic function connected in front of each of the row outputs.

However, Duwaer et al. in the same field of endeavor teaches logic function (i.e. 61-63 having h logic) is connected in the row drive circuit (row scanner) in front of each of row outputs (i.e. g₀-g_e) (see Fig. 2, Fig. 9, column 4, lines 43-44, and column 8, lines 41-55).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of invention to incorporate a method of logic function as taught by Duwaer in to the display system of He so that a logic function could be connected in front of each of the row outputs wherein the logic function deactivates/activates the row outputs in dependence on the partial mode responsive to a first control signal. In this configuration the system would have compact size and improve driving circuit for accurate data transmission in the display device (Duwaer, column 3, lines 67-68, column 4, lines 1-10).

(2) Regarding claim1:

He teaches a circuit arrangement for controlling a display device (150) which can be operated in a partial mode (column 1, lines 53-61), the circuit arrangement comprising a row drive circuit (140) for driving n rows (141-149) of the display device (150) and a column drive circuit (130) for driving m (131-139) columns of the display device, wherein the row drive circuit (140) controls the n rows (141-149) of the display device sequentially from 1 to n (141-149), and the column drive circuit (130) supplies column voltages to the m columns (131-139), which the column voltages correspond to the picture data to be displayed of pixels of the controlled row, characterized in that a

logic function (i.e. having logic zero) a first control signal (i.e. microprocessor 190 sends control signal pulse on a line control 105 via control circuit 130 via reset line 113 and reset low logic signal '0') is supplied, said first control signal (113) achieving a deactivation/activation (a fraction of display that can be turn off by the controller 110 which is connected to the row driver 140 turn, see column 3, lines 3-7) of the at least one row output (out put to the row lines 141-149) in dependence on the partial mode (partial display mode activating area) (column 2, lines 41-46, column 3, lines 1-30, fig. 1 and 2).

Note that He does not teach logic function is included in the row drive circuit in front of at least one row.

However, Duwaer et al. in the same field of endeavor teaches logic function (i.e. h logic) is included in the row drive circuit (row scanner) in front of each of at least one row (i.e. $g_0 - g_e$) (see Fig. 2, Fig. 9, column 4, lines 43-44, and column 8, lines 41-55).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of invention to incorporate a method of logic function as taught by Duwaer in to the display system of He so that the logic function could be included in the row drive circuit in front of at least one row output to which logic function a first control signal being supplied the first control signal achieving a deactivation/activation of the at least one row output in dependence on the partial mode. In this configuration the system would have In this configuration the system would have compact size and improve

driving circuit for accurate data transmission in the display device (Duwaer, column 3, lines 67-68, column 4, lines 1-10).

(3) Regarding claim 2:

Duwaer discloses that the logic function is connected in front of each row output (see Fig. 2, Fig. 9, column 4, lines 43-44, and column 8, lines 41-55).

(4) Regarding claim 3:

Duwaer teaches that the logic function (i.e. 61-63 being) being realized as an AND Gate (see Fig. 9).

(5) Regarding claim 5:

He teaches that the first control signal (113) is capable of switching (reset from 'on' state to 'off' state) off all n row outputs (cleared of data) by means of the logic functions (220, 2300) during the control (control by the control circuit 110) of a line that is not to be displayed in the partial mode (note that When the full display is active, both control lines 111, 118 are pulled low (logic zero). Using AND logic gates 220, 230 connected using lines 225, 235 to the inputs of an XOR logic gate 240, a reset signal is created on reset line 113 (control by 110) based on the number of lines that have already been activated and the partial display control signals (i.e, screen has partial data) When the reset line 113 goes low, the shift registers of the column drivers 130, shown in FIG. 1 are cleared of data. By resetting the row and column drivers before the full display has been activated (column 3, lines 12-30).

(6) Regarding claim 6:

He teaches that a control logic (i.e. signal 113) in the column drive circuit

(130) generates the first control signal in dependence on the partial mode and supplies the first control signal to the row driver circuit (140) (column 2, lines 41-46, column 3, lines 1-30, fig. 1).

(7) Regarding claim 7:

He teaches that the column drive circuit (130) supplies no column voltages to the m columns outputs (output to the data line 131 -139) in a case of a line that is not to be displayed (when the full display is active, both control lines 111, 118 are pulled low (logic zero). Using AND logic gates 220, 230 connected using lines 225, 235 to the inputs of an XOR logic gate 240, a reset signal is created on reset line 113 based on the number of lines that have already been activated and the partial display control signals; note that display portion or lines are controlled by a driving column voltage when the display portion is showing by lines in the display and driving in a manner that if there is no column voltage in certain lines, no display is available in that lines because pixel in a row occurred when voltage is applied to that pixel ; which means no column voltage is driving to the line in the case of a line that not to be displayed) (also see column (column 3, lines 12-30).

(8) Regarding claim 10:

He teaches that a display device (150) comprising a circuit arrangement (column 2, lines 41-46, column 3, lines 1-30 and Fig. 1 - 2).

(9) Regarding claim 11:

He teaches an electronic appliance (circuit) display device (150) (column 2, lines 41-46, fig 2-4).

(10) Regarding claim 12:

Note the discussion of He above in claim 1 which is similar to claim 12. Only the different, claim 1 is an apparatus and claim 12 is a method claim.

4. Claims 4 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over He in view of Duwaer as applied to claim 1 and further in view of Sarrasin et al. (US Patent No:5600343).

(1) Regarding claim 4:

Note the discussion of He above. He teaches that the row driver circuit (140) comprise a shift register (column 3 lines 43-45), but He does not teach that the shift register has n stages and n outputs, and in that a second control signal can be supplied to the shift register at the input thereof for controlling the consecutive rows 1 to n, which second control signal activates the outputs of the shift register consecutively in dependence on a clock signal.

However, Sarrasin in the same field of endeavor discloses the shift register (30) has n stages (32₁-32_i) and n outputs (output at (34₁-34_i)) and in that a second control signal (D) can be supplied to the shift register at the input (input data signal) thereof for controlling the consecutive rows (L1-Li), which second control signal activates the outputs (output at (34₁-34_i)) of the shift register (30) consecutively in dependence on a clock signal (Cp) (column 5, lines 43-67, fig. 3).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of invention to incorporate the shift register (30) which has n stages (32₁-32_i) and n outputs (output at (34₁-34_i)) and in that a second control signal (D) can be supplied to the shift register at the input (input data signal) as taught by Sarrasin in to the display system of He as modified by Duwaer so that for controlling the consecutive rows, which

second control signal activates the outputs of the shift register consecutively in dependence on a clock signal . In this configuration the system would be provided a significant reduction of the electrical consumption as a function of the image to be displayed (Sararsin, column 3, lines 61-63).

(2) Regarding claim 8:

Sarrasin teaches that the frequency of the clock signal (Cp) can be increased in the case of one or several consecutive rows (unused rows) that is or are not to be displayed (note that for each rising of the clock Cp the position of logic level '1' is on D then a logic '0' for all following clock stork. It should be noted that '0' is corresponds to the unselected rows, therefore, frequency of the signal will be increased in a manner that frequency of the clock Cp can be increased when the respective row line is turning off for the deactivateor partial turning off position (see column 6, lines 17-35).

Response to Arguments

5. Applicant's arguments, with respect to claim 1-12 have been considered but are moot in view of the new ground(s) of rejection.

6. In view of amendment the reference of Duwaer (US Patent No: 4922240) hasbeen added.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's discloser.

Inquiry

8. Any inquiry concerning this communication should be directed to the examiner at (571) 270-1673 Monday- Friday 7:30 AM to 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen, can be reached at (571) 272-7772.

Information regarding the status on an application may be obtained from the Patent Application information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

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Any response to this action should be mailed to:

Commissioner of patents and trademarks
Washington, D.C. 20231

Or fax to:

(703)872-9314 (for Technology Center 2600 only)

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SUPERVISORY PATENT EXAMINER